REMARKS

Claim Rejections

Claims 1-6 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 1-6 are rejected under 35 U.S.C. § 102(e) as being anticipated by Nishii (US 6,698,093).

New and Amended Claims

By this Amendment, Applicant has canceled claim 1 and has added new claim 13 to this application. Claims 2-6 have been amended to depend from new claim 13. Claim 5 has also been amended to correct an idiomatic error. It is believed that the new and amended claims specifically set forth each element of Applicant's invention in full compliance with 35 U.S.C. § 112, and define subject matter that is patentably distinguishable over the cited prior art, taken individually or in combination.

The new claims are directed toward: a method of forming a multi-layer printed circuit board (PCB), said multi-layer PCB including one or more cores, a plurality of circuit layers formed by using a resin build-up process or a lamination process to increase the number thereof, said method comprising: forming with said resin build-up process a resin layer as a first dielectric layer (e.g., 4 in Fig. 2 and 15 in Fig. 3) of inner circuit layers (e.g., 1a, 1b, 3a, 3b, 5a, and 5b in Fig. 2 and 12a, 12b, 13a, 13b, 14a, 14b, and 15) of said multi-layer PCB; forming on said resin layer a circuit layer as one o inner circuit layer for refinement of circuits thereon; and forming a second dielectric layer (e.g., 6 in Fig. 2; 16 and 16a in Fig. 3) as an outer circuit layer (e.g., 7a, 7b, 6 in Fig. 2 and 11a, 11b in Fig. 3) formed with said lamination process to enhance a thermal resistance, a copper peel strength, a stiffness, and a thermal stress reliability of said outer circuit layer.

That is, the main characteristic and the primary function of the invention is that said circuit layers located at inner and outer layers of said multi-layer PCB are specifically limited to be formed with said resin build-up process and said lamination process, respectively.

Currently there are many prior types of processes used to form multiple layers, but most multi-layer printed circuit boards are manufactured with only one

type of process to form multiple layers, such as in a VIL process developed by JVC of Japan, i.e., liquid epoxy coating is employed to form the inner and the outer circuit layers of the multi-layer PCB. That is, both the outer and the second and third inner circuit layers are formed with the ***same*** resin build-up process. *See* BACKGROUND or page 5, 6 of the specification of the invention. Further, Nishii discloses in Fig.3 a multilayered PCB having prepregs and circuits; epoxy comes in stages A, B or C and can be built-up and laminated depending on the stages of the epoxy. Nishii also discloses a variety of epoxy processes and further discloses aramid fiber as described in USPTO DETAILED ACTION page 4, line 1-3. That is, Nishii discloses a prepreg material or an aramid fiber material or an epoxy material formed as a dielectric layer of a multi-layer PCB. Therefore, Nishii only generally discloses that the dielectric layer and the circuit layer of a multi-layer PCB may be formed from different dielectric material and with different process. However, Nishii does not disclose or teach that an inner layer of a multi-layer PCB is specifically limited to be formed from a resin material as a dielectric and with said resin build-up process, and the outer layer of said multi-layer PCB is especially limited to be formed from a laminating dielectric with said lamination process, as recited by Applicant.

Currently, many types of processes are used to form multiple layers of a multi-layer PCB, including resin build-up processes and lamination processes. That is, the steps as disclosed in the fifth step shown in Fig. 2E to the eighth step shown in Fig. 2H for forming the multi-layer PCB 100 of Fig. 1 are known as a ***resin build-up process***, and the steps as disclosed in the ninth step shown in Fig. 2I to the tenth step shown in Fig. 2J for forming the multi-layer PCB 100 of Fig. 1 are known as a prior art of ***lamination process***. Moreover, the above-mentioned steps shown in Figs. 2A to 2K, operations including laminating, liquid epoxy coating, dry film type epoxy laminating, laser drilling, mechanical drilling, copper plating, etching, and applying solder mask, are also known as the prior art in the related technical field of PCB.

Applicant's improvement is formulating a process which combines, **on the same PCB** both a resin build-up process for an inner layer and a lamination process for an outer layer. For instance, for the purpose of the 8-layer PCB 100 of Fig. 1, the circuit layers 7a and 7b are the outer circuit layers that form a first layer of the PCB

100, while the circuit layers 1a and 1b, 3a and 3b, and 5a and 5b shall be referred to as the inner circuit layers. Wherein, the inner circuit layers 5a and 5b and the inner circuit layers 3a and 3b form a second and a third layer, respectively, of the PCB 100, and are the second and the third inner circuit layer, respectively. The present invention is characterized in that the resin build-up process and the lamination process are employed to form the inner circuit layers and the outer circuit layers, respectively, of the 8-layer PCB 100. More specifically, the inner circuit layers, such as the second inner circuit layers 5a and 5b, which require the refinement of circuits are formed by using a resin material, such as epoxy, as the dielectric to form the resin layers 4 with the resin build-up process through liquid epoxy coating or dry film type epoxy laminating, and then forming the inner circuit layers 5a and 5b. Thereafter, the dielectric layers 6 using the prepreg or the aramid fiber material as the dielectric and the outer circuit layers 7a, 7b are formed with the lamination process.

By using the resin build-up process and the lamination process to form different layers on the same one multi-layer PCB, the completed multi-layer PCB 100 is able to include advantages obtainable from the two processes. For example, the second inner circuit layers 5a and 5b of the multi-layer PCB 100 formed with the resin build-up process possesses improved circuit refinement to satisfy the circuit design requirements of the multi-layer PCB, while the outer circuit layers 7a and 7b of the multi-layer PCB 100 formed with the lamination process have improved thermal resistance, copper peel strength, stiffness, thermal stress reliability, and size stability. Therefore, the fully completed 8-layer PCB 100 is superior as compared to a multi-layer PCB formed with only one of the conventional forming processes. Therefore, Applicant's recited invention is clearly not taught by the cited prior art of Nishii.

Nishii does not teach: a method of forming a multi-layer printed circuit board (PCB), said multi-layer PCB including one or more cores, a plurality of circuit layers formed by using a resin build-up process or a lamination process to increase the number thereof, said method comprising: forming with said resin build-up process a resin layer as a first dielectric layer of said inner circuit layers of said multi-layer PCB; forming on said resin layer a circuit layer as one of said inner circuit layer for

refinement of circuits thereon; and forming a second dielectric layer as an outer circuit layer formed with said lamination process to enhance a thermal resistance, a copper peel strength, a stiffness, and a thermal stress reliability of said outer circuit layer.

It is axiomatic in U.S. patent law that, in order for a reference to anticipate a claimed structure, it must clearly disclose each and every feature of the claimed structure. Applicant submits that it is abundantly clear, as discussed above, that Nishii do not disclose each and every feature of Applicant's new claims and, therefore, could not possibly anticipate these claims under 35 U.S.C. § 102. Absent a specific showing of these features, Nishii cannot be said to anticipate any of Applicant's new claims under 35 U.S.C. § 102.

It is further submitted that Nishii do not disclose, or suggest any modification of the specifically disclosed structures that would lead one having ordinary skill in the art to arrive at Applicant's claimed structure. Thus, it is not believed that Nishii render obvious any of Applicant's new claims under 35 U.S.C. § 103.

Summary

In view of the foregoing amendments and remarks, Applicant submits that this application is now in condition for allowance and such action is respectfully requested. Should any points remain in issue, which the Examiner feels could best be resolved by either a personal or a telephone interview, it is urged that Applicant's local attorney be contacted at the exchange listed below.

Respectfully submitted,

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